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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,156	10/25/2001	James D. Beasom	125.020US01	7041

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,156	BEASOM, JAMES D.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 2, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Nordstom et al. (US 2001/0012655 A1).

3. Regarding Claim 1,Nordstom et al. disclose a process for producing an integrated circuit comprising the steps of forming a nitride sealing layer (first layer) (25) (Figure 18) in a contact opening, wherein a second layer of nitride (44) (Figure 25a) is formed (page 13, [0137]) overlaying the first nitride layer and without any intervening layers between the first and second nitride layers (See Region 18 and 5, Figure 25a) (Figure

25a) to form a sealing layer, and further overlaying an exposed portion of the substrate and sidewalls of the opening. Using RIE (page 13, [0140],[0138]) without an external mask, a portion of the second nitride layer is removed to expose the surface of the substrate without removing portions of the nitride covering the sidewalls (Figure 25b).

4. Regarding Claim 2, Nordstom et al. disclose (page 13, [0139]) that the nitride layer is deposited by LPCVD.

5. Regarding Claim 4, Nordstom et al. disclose (Figure 25b) that a portion of the first nitride layer (34) (under poly-Si 38) remains overlying the oxide ("edge of T-shaped region above well) after RIE ([0138],[0140]) is applied.

Claim Rejections – 35 U.S.C. 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstom et al., as applied to Claim 1, and further in view of Wu (US 5,679,601).

Nordstom et al. do not disclose that the second nitride layer is formed by plasma enhanced chemical vapor deposition (PECVD). However, Wu discloses that PECVD (Col. 3,

lines 66 – 67, Col.4, lines 1 – 5) is used to form the second sealing nitride layer (22) (Figure 6) and the layer etched by RIE to form sidewall spacers (Figure 7). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wu and Nordstom et al. to obtain a PECVD nitride layer of controlled density to reduce indiffusion of contaminants to the active device area.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstom, as applied to Claim 1.

Nordstom et al. disclose the use of RIE for etching the nitride layer, but do not disclose the times required to perform the task of removing the nitride overlaying the surface of the substrate without removing portions of the nitride layer overlaying portions of the sidewalls. It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the times of etch to avoid removing all of the layer from sidewalls. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimal or working ranges involves only routine skill in the art In re Aller, 105 USPQ 233.

9. Claims 7 - 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstom et al.

10. Regarding Claim 7, as discussed previously, Nordstom et al. disclose a process for producing an integrated circuit where an oxide is formed on the surface of a substrate, wherein a first layer of nitride is formed overlaying the oxide in a contact opening formed in the integrated circuit. A second layer of nitride is deposited (page 13, [0137]) over the

first nitride layer, further overlaying an exposed portion of the substrate and sidewalls of the opening (Figure 25a). Using RIE (page 13, [0140], [0138]) without an external mask, a portion of the second nitride layer is removed to expose the surface of the substrate without removing portions of the nitride covering the sidewalls (Figure 25b) where the overlaying nitride layers seal the oxide("edge of T-shaped region above well).

11. Regarding Claim 8, Nordstom et al. disclose (page 11, [0128]) that the contact openings through the nitride and oxide layers are done with a dry etch with one photoresist mask (Figure 21b).

12. Regarding Claim 9, Nordstom et al. disclose (page 8, [0105]) the formation of a thermally grown oxide layer.

13. Regarding Claim 10, Nordstom et al. disclose that functional devices within the integrated circuit are formed with a thermal oxide as the interfacial layer, but do not disclose that the oxide layer is "deposited." The formation of oxide layers by deposition is extremely well known in the art and commercial equipment readily available (for example, Applied Materials, Novellus, Lam Research and others). Therefore, it would have been obvious to one of routine skill in the art at the time of the invention to utilize deposited films of oxide.

14. Regarding Claim 11, Nordstom et al. disclose that the first nitride layer is formed by LPCVD (page 8, [0105]) and that the second nitride layer is formed by LPCVD (page 13, [0137]).

15. Regarding Claim 12, Nordstom et al. disclose that functional devices within the integrated circuit are formed with LPCVD nitride layers. It would be obvious that PECVD could also be used to form the first and second layers of nitride, since both techniques produce a layer by CVD. In addition, commercial machines (Applied Materials,Novellus) are readily available in the art for plasma enhanced deposition. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form both nitride layers by PECVD.

16. Regarding Claim 13, Nordstom et al. disclose (Figure 25b) that a portion of the first nitride layer remains overlying the oxide (See area near interface of area 13) after RIE is applied.

17. Claims 14 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstom et al. in view of S. Wolf and R.N. Tauber, ("Silicon Processing for the VLSI Era: Volume 1 – Process Technology," Lattice Press, sunset Beach, CA (1986), pp. 321 – 324).

18. Regarding Claim 14, Nordstom et al. disclose a method for forming semiconductor devices in an integrated circuit with a plurality of device types in a substrate at the surface of the substrate having regions doped to a first conductivity type (page 21, claim 40). An oxide layer is grown over the substrate and subsequently patterned to expose pre-selected portions of the substrate (Figure 7). Ion implantation (second conductivity type) is done through a thin oxide that serves as stopping layer to define edge zones (Figure 8). A nitride layer is formed on the oxide and masked to define device areas

(Figure 14) of the first and second conductivity type. A second layer of nitride is deposited (page 13, [0137]) over the first nitride layer, further overlaying an exposed portion of the substrate and sidewalls of the opening Using RIE (page 13, [0140], [0138]) a portion of the second nitride layer is removed to expose the surface of the substrate without removing portions of the nitride covering the sidewalls (Figure 25b), wherein the oxide layer (edge of T – shaped region) remains sealed by the first and second layers of nitride. Nordstrom et al. disclose the use of RIE for etching the nitride layer, but do not disclose the times required to perform the task of removing the nitride overlaying the surface of the substrate without removing portions of the nitride layer overlaying portions of the sidewalls. It would have been obvious to one of ordinary skill in the art at the time of the invention to adjust the times of etch to avoid removing all of the layer from sidewalls. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimal or working ranges involves only routine skill in the art In re Aller, 105 USPQ 233.

Nordstom et al. do not use a nitride film as part of a two-layer stopping layer structure for ion implantation, but rather a single layer oxide film. Thin oxide and nitride films are equivalent for ion implant stopping layers and have been used in the art since the early 1970's. It is well known in the art that nitride and oxide have equivalent "stopping" capability for ions, based on cross sections (See for example, S. Wolf and R.N. Tauber, pp. 321 – 324) and the physical effects are similar. Hence, based on equivalence and widely known use in the art, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a nitride stopping layer atop the oxide for accelerating process flow, since the two dielec-

trics are approximately equivalent in stopping power. Further, a first nitride layer is deposited atop the oxide layer, subsequent to ion implantation, followed by formation of a second nitride layer, whereby the layer sequence is sealed.

19. Regarding Claim 15, Nordstom et al. disclose (page 11, [0128]) that the contact openings through the nitride and oxide layers are done with a dry etch with one photo-resist mask (Figure 21b).

20. Regarding Claim 16, Nordstom et al. disclose that the first nitride layer is formed by LPCVD (page 8, [0105]) and that the second nitride layer is formed by LPCVD (page 13, [0137]).

21. Regarding Claim 17, Nordstom et al. disclose that functional devices within the integrated circuit are formed with LPCVD nitride layers. It would be obvious that PECVD could also be used to form the first and second layers of nitride, since both techniques produce a layer by CVD. In addition, commercial machines (Applied Materials, Novellus) are readily available for plasma enhanced deposition. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form both nitride layers by PECVD.

22. Regarding Claim 18, Nordstom et al. disclose (Figure 25b) that a portion of the first nitride layer remains overlying the oxide after RIE is applied (See near left side interface of Area 13, edge of T-shaped region).

Response to Arguments

23. Arguments of Applicant with regard to Claims have been carefully considered, but have not been found to be persuasive. With regard to Claim 1(page 6, Response) there are no intervening layers between the first and second layers in forming the "sealing" nitride (at edges, Figure 25a, layers 44 and 34), analogous to Figure 3F of the instant application, where nitride layer 160 seals layer 106 and 102 (Specification, para. [0027]) at the edges. Hence, the reference reads clearly on the limitations of Claim 1.

With regard to Claim 4 (pages 6 – 7, Response), Applicant is incorrect. RIE is applied ([0137] and [0140] until the oxide is removed in the opening, leaving the portion of oxide (at T-region with oxide portion extending laterally) underlaying the nitride layer. This issue has been addressed in detail in previous Office Actions.

With regard to Claim 7 (pages 7 – 9, Response), Applicant is incorrect in asserting that a "mask" is used. There is no external mask used in the reference. The lateral spacers (45) are a part of the structure and used functionally to decrease and control removal, analogous to layer 160 serving as an internal mask for removal (Figures 3E and 3F) control in the instant application. As discussed above, and in previous Office Actions, RIE is applied until the substrate is exposed in the opening ([0137], [0140]), with the oxide(T-shaped region with oxide portion extending laterally) "sealed" by the nitride layers. The reference contains all of the limitations in the claim of the instant application.

With regard to Claim 14, (pages 9 – 10, Response), the equivalence of "stopping layers has been discussed in detail in the previous Office Action. Applicant is reminded that the

oxide layer is also used in the instant application as a stopping layer, as part of a two layer structure consisting of oxide and nitride, which now forms the "effective stopping layer." Since oxide and nitride are approximately equivalent in stopping power, it would be trivial to add an extra thickness of nitride on the oxide of Nordstrom. The motivation for so doing is indeed a strong one, i.e., to improve process efficiency and reduce costs in the device fab flow.

Conclusions

24. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
February 12, 2004